AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

Claims 1-24. (Canceled)

25. (New) Dynamic Nonvolatile Random Access Memory for storing information, comprising a one-transistor cell having a control gate, a floating gate and source and drain terminals wherein a silicon carbide device is disposed between the control gate and the floating gate and information is read by sensing resistance between the source and drain terminals of the transistor.

26. (New) Dynamic Nonvolatile Random Access Memory as claimed in claim 25 in which the silicon carbide device is an isolation diode.

27. (New) Dynamic Nonvolatile Random Access Memory as claimed in claim 26 in which the silicon carbide is a 3C SiC wafer.

28. (New) Dynamic Nonvolatile Random Access Memory as claimed in claim 26 in which said isolation diode is implemented in silicon carbide with SiO_2 as the insulator and the SiC-SiO_2 interface is passivated to create charge retention times sufficiently long to avoid the need for the one trasnsitor memory cell to be electrically refreshed.

29. (New) Dynamic Nonvolatile Random Access Memory as claimed in claim 28 in which the charge retention times are greater than 7 years.

30. (New) Dynamic Nonvolatile RAM as claimed in claim 28 in which the SiC-SiO_2 interface is nitrided in either NO or N_2O rich environments.

31. (New) Dynamic Nonvolatile RAM as claimed in claim 28 in which the $SiC\text{-}SiO_2$ interface is prepared by direct oxide growth or by annealing of pre-grown oxide on the SiC layer in the presence of NO or N_2O.

32. (New) The dynamic NVRAM as claimed in claim 26 wherein the isolating diode is a reference-type diode with both forward and reverse on operation when the forward and reverse turn-on voltages are exceeded.

33. (New) A method of fabricating an NVRAM as claimed in claim 31 which includes the step of forming a nitrided silicon oxide gate on the silicon carbide substrate and subsequently carrying out ion implantation.

34. (New) A one transistor cell for use as a memory device for storing information, said cell having a control gate, a floating gate and source and drain terminals wherein a silicon carbide device is disposed between the control gate and the floating gate and information is read by sensing resistance between the source and drain terminals of the transistor.

35. (New) A one transistor cell as claimed in claim 34 in which the silicon carbide device is an isolation diode.

36. (New) A one transistor cell as claimed in claim 34 in which the silicon carbide device includes SiO_2 as an insulator and a resulting $SiC\text{-}SiO_2$ interface is passivated to create charge retention times sufficiently long to avoid the need for the one transistor memory cell to be electrically refreshed.

37. (New) A one transistor cell as claimed in claim 26 in which the $SiC\text{-}SiO_2$ interface is nitrided in either NO or N_2O rich environments.

38. (New) A one transistor cell as claimed in claim 36 in which the SiC-SiO_2 interface is prepared by direct oxide growth or by annealing of pre-grown oxide on the SiC layer in the presence of NO or N_2O.

39. (New) A one transistor cell as claimed in claim 36 in which source and drain contacts are used to sense resistance and the resistance depends on the electric field formed by the nonequlibrium charge stored at the floating gate.

40. (New) A one transistor cell as claimed in claim 39 in which metal or heavily-doped polysilicon are used for the drain and source contacts.

41. (New) A one transistor cell as claimed in claim 35 in which the isolation diode is created from N-type and P-type semiconductors forming either NPN or PNP structures.

42. (New) A random-access memory array in which memory cells as claimed in claim 34 are connected by word lines connecting control gates, the word lines are in parallel with source lines connecting the source contacts, and the word and source lines are crossing bit lines that connect the drain contacts.